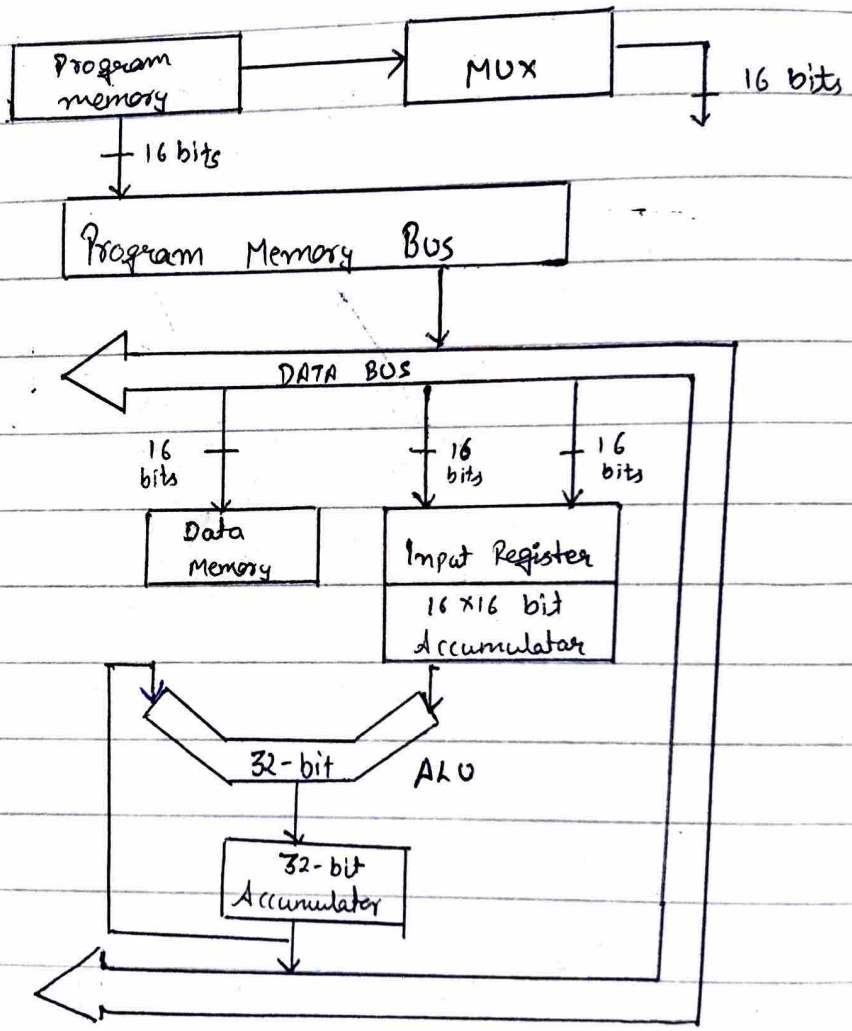
Q Discuss basic architecture of TMS series of digital signal processor.

Ans The TMS 320 Cxx Series of DSP processor is manufactured by Texas Instruments.

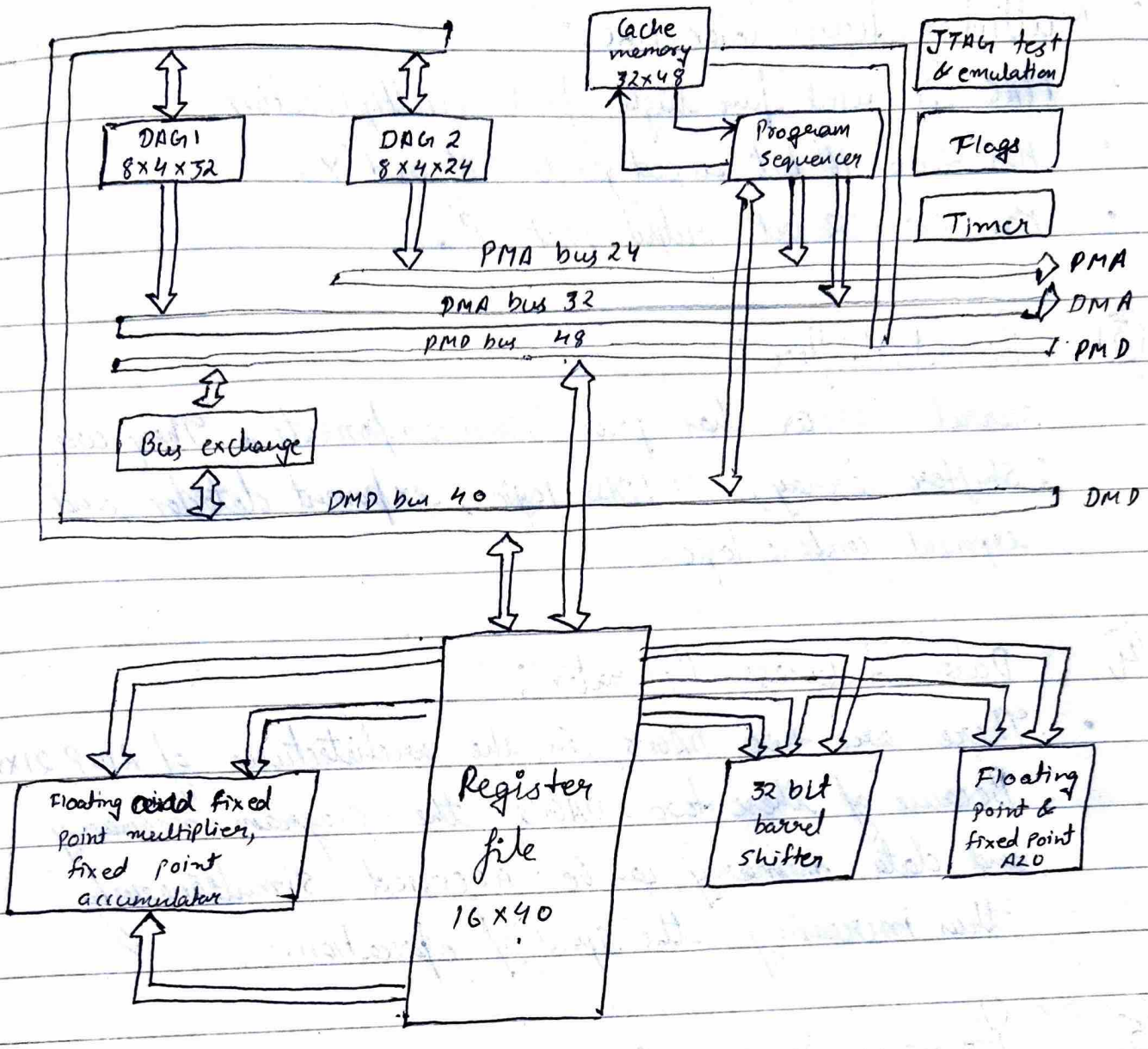
(i) TMS 320 C_{10} (1st generation)



1st generation DSP processor was introduced in 1982

Key features include:

Arithmetic unit: which includes multiplexer, accumulator and shifter. This processor family has modified Harvard architecture with two separate memory space for program and data. It has on chip memory and special instructions for execution of basic DSP algorithm



① Arithmetic logic Unit (ALU) :-

Performance of ALU is same as any processer performing logical as well as arithmetic functions.

- It is 16 bit wide
- It has two input ports X and Y
- It has one output port R
- ALU generates six status signal and one CI (carry In) bit which are stored in ASTAT (arithmetic status) register.

② Multiplier Accumulator MAC:

- MAC is used for high speed multiplication
- Has two 16 bit input ports 'x' and 'y'.
- Has one 32 bit output port 'P'.

③ Barrel Shifter:

- Barrel shifter has four main components. They are : shifter array, OR/PASS logic, exponent detector and exponent compare logic.

④ Data Address Generater:

- There are two DAG's in the architecture of ADSP 21XX.
- Because of these two DAG's the program memory and data memory can be accessed simultaneously thus increasing the speed of operation.

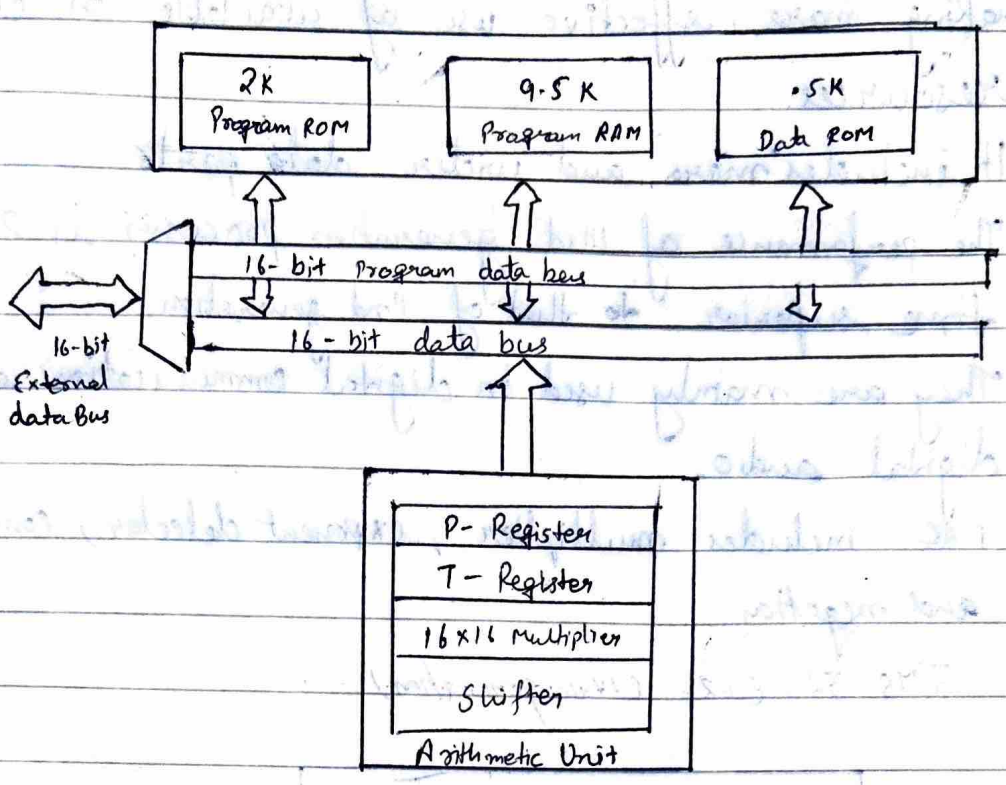
⑤ Program Sequencer:

- It generates addresses for the instructions.
- It provides flexible control of the program flow.
- It gives sophisticated interrupt processing.
- Conditional as well as unconditional zero overhead looping is provided.

⑥ Cache Memory:

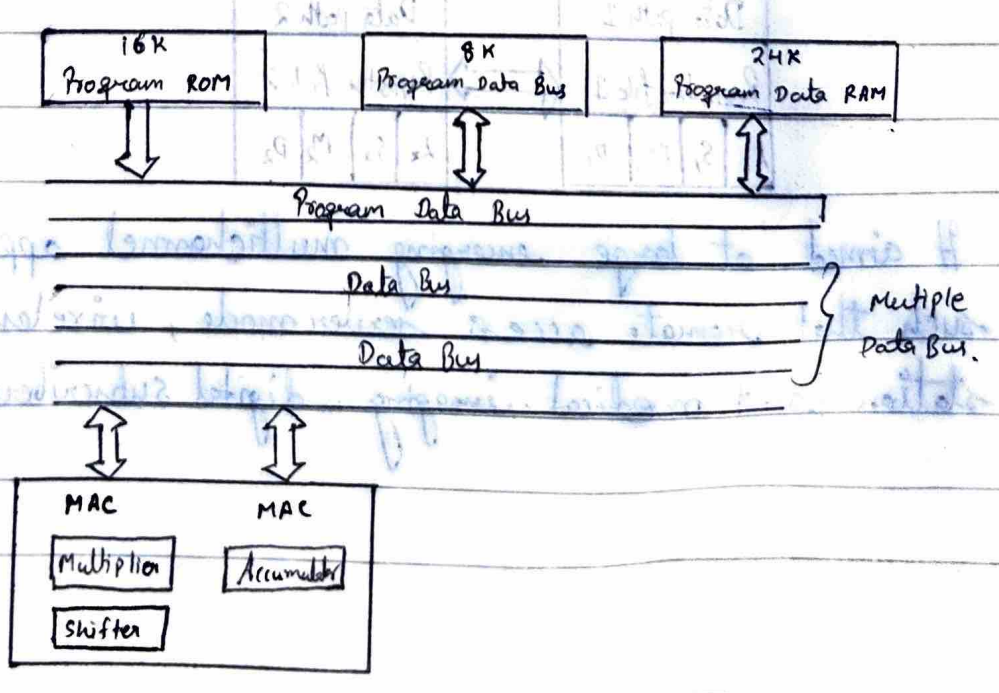
- In computer science it is a short-term memory in a computer with quick access.
- A cache is intended to speed up access to a set of data.

(ii) TMS 320 C50 (IInd generation)



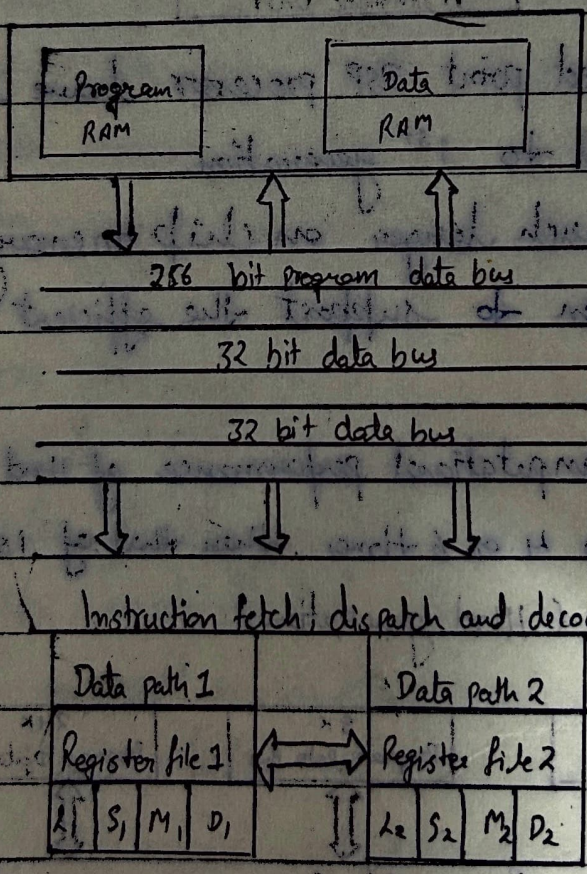
- IInd generation fixed point DSP processor have enhanced features compared to 1st generation.
- There include much larger on chip memory and more special instruction to support the efficient execution of DSP algorithm.
- As a result computational performance of IInd generation DSP processor is 4 or 6 times than that of 1st generation.

(iii) TMS 320 C54 (IIIrd generation)



- In this the performance enhancement is increased or making more effective use of available on chip resources.
→ It includes more and wider data parts
→ The performance of IIIrd generation processor is 2 or 3 time superior to that of IInd generation.
→ They are mainly used in digital communication and digital audio.
→ MAC includes multiplier, exponent detector, comparison and negation.

(iv) TMS 320 C62 (IV th generation)



→ It aimed at large emerging multichannel applications such that remote access server mode, wireless base station and medical imaging, digital subscribers loop etc.

→ It includes two independent arithmetic parts each with 4 execution units i.e logic unit, shifter, multiplier and data address unit.

→ It has a large program and data cache memory, each part has its own register file but it can also access register on other data parts.